TITLE OF THE INVENTION

DISPLAY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a display device, and more particularly, to an active-matrix type liquid crystal display device which forms a liquid crystal display driving circuit on the liquid-crystal-side surface of one of substrates which are arranged to face each other with liquid crystal therebetween.

2. Description of the Related Art

Among display devices, an active-matrix type display device defines pixel regions on a liquid-crystal-side surface of one of the transparent substrates which are arranged to face each other with liquid crystal therebetween, wherein the pixel regions are surrounded by gate signal lines which are extended in the x direction and are arranged in parallel in the y direction and drain signal lines which are extended in the y direction and are arranged in parallel in the x direction.

Then, each pixel region is provided with a thin film transistor which is driven by scanning signals from a gate signal line on the one hand and a pixel electrode to which video signals are supplied from a drain signal line on the other hand through that thin film transistor.

These pixel electrodes generate an electric field between the pixel electrode and the counter electrode which is formed opposite it on the liquid-crystal-side surface of the other transparent substrate having intensity which corresponds to the video signal, so as to control the light transmittivity of the liquid crystal.

Further, as the liquid crystal display device having the above constitution, there has been known a liquid crystal display device which also comprises a scanning signal driving circuit and a video signal driving circuit for respectively supplying signals to respective gate signal lines and respective drain signal lines on the other transparent substrate on the side facing the liquid crystals. Each circuit is comprised of a large number of MIS (Metal-Insulator-Semiconductors) type transistors having a constitution similar to that of the thin film transistor in the pixel region. These circuits can be formed simultaneously with the formation of the pixels.

In this case, polycrystalline silicon (Poly-Si) has been used as semiconductor layers of the thin film transistor and the MIS type transistor.

However, with respect to the display device having such a constitution, when the liquid crystal display device is used as a display device of a portable telephone, an inconvenience that the power consumption is relatively large has been pointed

out.

Further, since a video signal driving circuit uses a dynamic memory, there has been an inconvenience that a leak current flows into the thin film transistor which constitutes the dynamic memory.

Further, it has been also pointed out that when the dynamic memory generates photons in a semiconductor layer due to light from the outside, the inconvenience brought about by the photon gives rise to more adverse influence than the thin film transistor formed in the inside of the pixel region, for example.

SUMMARY OF THE INVENTION

The present invention has been made in view of such circumstances and it is an object of the present invention to provide a display device which can minimize the power consumption.

It is another object of the present invention to provide a display device which can suppress a leak current which is generated in thin film transistors which constitute a dynamic memory in the inside of a video signal driving circuit.

It is still another object of the present invention to provide a display device which can normally operate the dynamic memory in the video signal driving circuit.

To briefly explain the summary of typical inventions

among inventions which are disclosed in the present application, they are as follows.

Means 1

A display device is characterized in that

gate signal lines which are extended in the x direction and are arranged in parallel in the y direction, scanning signal driving circuits which supply scanning signals to respective gate signal lines, drain signal lines which are extended in the y direction and are arranged in parallel in the x direction, and video signal driving circuits which supply video signals to respective drain signal lines are formed on one of substrates on the surface facing the liquid-crystals which are arranged to face each other in an opposed manner with liquid crystal between them,

the display device includes a thin film transistor which is driven by the scanning signals from one side of the gate signal line, and a pixel electrode to which the video signals from one side of the drain signal line are supplied through the above thin film transistor in each pixel region which is surrounded by the respective signal lines,

a display region which is a collection of the above pixel regions is distinguished from the other display regions using imaginary lines extending along the x direction as boundaries,

the scanning signal driving circuit which supplies the scanning signals to respective gate signal lines in one display

region and the scanning signal driving circuit which supplies the scanning signals to respective gate signal lines in the other display region are separately formed,

the drain signal lines at one display region are separated from the drain signal lines at other display regions, and

the video signal driving circuit which supplies the video signals to respective drain signal lines in one display region and the video signal driving circuits which supply the video signals to respective drain signal lines in other display region are separately formed.

In the display device having such a constitution, although one display region and another display region can be used as a single display region, it becomes possible to use only either one of these display regions for display.

Accordingly, it is unnecessary to supply the scanning signals to the display region which is not used for display so that the power consumption can be reduced.

Means 2

A display device is characterized in that

gate signal lines which are extended in the x direction and are arranged in parallel in the y direction, a scanning signal driving circuit which supplies scanning signals to respective gate signal lines, drain signal lines which are extended in the y direction and are arranged in parallel in the

x direction, and a video signal driving circuit which supplies video signals to respective drain signal lines are formed on one of substrates which are arranged to face each other with liquid crystal inserted between them, on the surface of the substrate facing the liquid crystals.

the display device includes a thin film transistor which is driven by the scanning signals from one side of the gate signal line and a pixel electrode to which the video signals from one side of the drain signal line are supplied through that thin film transistor in each pixel region which is surrounded by the respective signal lines,

the video signal driving circuit includes a dynamic memory which is comprised of a plurality of other thin film transistors formed in parallel with the above-mentioned thin film transistor, and

at least one thin film transistor among a plurality of thin film transistors is covered with a conductive film having a potential which is fixedly secured by way of an insulation film.

The display device having such a constitution can increase the capacity in the thin film transistors which constitutes the dynamic memory so that the generation of a leak current can be suppressed.

Means 3

A display device is characterized in that

the display device includes a liquid crystal display panel and a backlight which is arranged at the rear of the liquid crystal display panel,

gate signal lines which are extended in the x direction and are arranged in parallel in the y direction, a scanning signal driving circuit which supplies scanning signals to respective gate signal lines, drain signal lines which are extended in the y direction and are arranged in parallel in the x direction, and a video signal driving circuit which supplies video signals to respective drain signal lines are formed on a one of substrates which are arranged to face each other in an opposed manner with liquid crystal inserted between them, on the side facing the liquid-crystal,

the display device includes a thin film transistor which is driven by the scanning signals from one side of the gate signal line and a pixel electrode to which the video signals from one side of the drain signal line is supplied through the thin film transistor in each pixel region which is surrounded by the respective signal lines,

the video signal driving circuit includes a dynamic memory which is comprised of a plurality of other thin film transistors formed in parallel with the above-mentioned thin film transistor, and

a light shielding film which prevents the backlight from irradiating the dynamic memory is formed on the substrate on

the side which faces the backlight.

The liquid crystal display device having such a constitution can shield the irradiation of an external light to the thin film transistors which constitutes the dynamic memory so that it becomes possible to operate the dynamic memory normally.

Further means and advantageous effects of the present invention will be apparent hereinafter in the following description including claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an overall equivalent circuit diagram showing one embodiment of a liquid crystal display device according to the present invention.

Fig. 2 is an equivalent circuit diagram showing one embodiment of a video signal driving circuit of the liquid crystal display device according to the present invention.

Fig. 3 is a plan view showing one embodiment of a pixel in the liquid crystal display device according to the present invention.

Fig. 4 is a cross-sectional view taken along a line IV-IV in Fig. 3.

Fig. 5 is a plan view showing one embodiment of a dynamic memory (1 bit) of the liquid crystal display device according to the present invention.

Fig. 6 is a cross-sectional view taken along a line VI-VI in Fig. 5.

Fig. 7 is an equivalent circuit diagram showing one embodiment of a dynamic memory of the liquid crystal display device according to the present invention.

Fig. 8 is an operation explanatory view of the dynamic memory of the liquid crystal display device according to the present invention.

Fig. 9 is a cross-sectional view showing one embodiment of the liquid crystal display panel according to the present invention.

Fig. 10 is an explanatory view showing one embodiment of a liquid crystal display driving method according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of a liquid crystal display device according to a present invention are explained in conjunction with attached drawings hereinafter.

«Overall constitution»

Fig. 1 is an scale circuit diagram showing one embodiment of a liquid crystal display device according to the present invention. Although the drawing is the circuit diagram, it is illustrated corresponding to the actual geometric arrangement.

In the drawing, first of all, there is shown a transparent

substrate SUB1. The transparent substrate SUB1 is arranged to directly face a transparent substrate SUB2 (not shown in the drawing) with liquid crystal inserted between them. The transparent substrate SUB 2 at least covers the liquid crystal display portion AR and is fixedly secured to the transparent substrate SUB1 using a sealing agent SL which also forms the periphery of the liquid crystal display portion AR (see Fig. 9).

In the drawing, on the transparent substrate SUB1 on the liquid crystal side, gate signal lines GL which are extended in the x direction and are arranged in parallel in the y direction and drain signal lines DL which are insulated from the gate signal lines GL, are extended in the y direction and are arranged in parallel in the x direction are formed.

Each rectangular region which is formed by a pair of respective gate signal lines GL and a pair of drain signal lines DL constitutes a pixel region. A collection of these pixel regions which are arranged in a matrix array constitutes the liquid crystal display portion AR.

Here, in this embodiment, the respective drain signal lines DL are formed such that they are divided at the center of the liquid crystal display portion AR. That is, the liquid crystal display portion AR is conceptually divided into the respective pixel regions which are formed of respective gate signal lines GL ranging from the gate line of the 1st row

constituting the uppermost edge to the gate line of the ith row (referred to as "front stage display portion ARf" hereinafter) and respective gate signal lines GL ranging from the gate line of the (i-1)th row line to the lowermost nth row line (referred to as "back stage display portion ARb" hereinafter). The drain signal lines DL which are in charge of the front-stage display portion ARf and the drain signal lines DL which are in charge of the back-stage display portion ARb are arranged such that they are electrically separated.

In this case, the value of "i" differs depending on the use of the liquid crystal display device and the "i" may be at the upper stage side with respect to the center of the liquid crystal display portion AR (the center in the y direction in the drawing) or may be at the lower stage side with respect to the center of the liquid crystal display portion AR.

Then, one side (the right side in the drawing) of the respective gate signal lines GL in the front-stage display portion ARf are connected to a pixel driving shift register 1f which constitutes the scanning signal driving circuit, while the pixel driving shift register 1f is driven by a start pulse clock signal supplied from outside the liquid crystal display device.

Further, one side (the right side in the drawing) of the respective gate signal lines GL in the back-stage display portion Arb are connected to a pixel driving shift register 1b

which is provided separately from the above-mentioned pixel driving shift register 1f, while this pixel driving shift register 1b is also driven by the above-mentioned start pulse clock signal.

Further, one side (the upper side in the drawing) of the respective drain signal lines DL in the front-stage display portion ARf are connected to the video signal driving circuit. The video signal driving circuit is comprised of a D-A converting circuit 2f, a memory 3f, an input data take-in (output) circuit 4f, and an H-side address decoder 5f which are sequentially arranged in parallel in this order starting from the drain signal line DL, and a V-side address decoder 6f and a memory driving shift register 7f which are connected to the memory 3f.

To the H-side address decoder 5f, the input data take-in (output) circuit 4f and the V-side address decoder 6f, a pixel address (H), pixel data and a pixel address (V), which are supplied from outside the liquid crystal display device, are respectively inputted.

Further, the memory driving shift register 7f is configured to be driven by inputting the above-mentioned start pulse clock signal.

A more detailed configuration of such a video signal driving circuit is shown in Fig. 2.

Further, one side (the lower side in the drawing) of the

respective gate signal lines GL in the back-stage display portion ARb are connected to a video signal driving circuit which is provided separately from the above-mentioned video signal driving circuit. This video signal driving circuit is, in the same manner as the above-mentioned video signal driving circuit, comprised of a D-A converting circuit 2b, a memory 3b, an input data take-in (output) circuit 4b, and an H-side address decoder 5b which arranged in parallel in order from the drain signal line DL side, and a V-side address decoder 6b and a memory driving shift register 7b which are connected to the memory 3b.

To the H-side address decoder 5b, the input data take-in (output) circuit 4b and the V-side address decoder 6b, a pixel address (H), pixel data and a pixel address (V) which are supplied from outside the liquid crystal display device are respectively inputted.

Further, the memory driving shift register 7b is configured to be driven by inputting the above-mentioned start pulse clock signal.

Then, electric power is supplied to the scanning signal driving circuits and the video signal driving circuits from outside the liquid crystal display device through a power supply control circuit 9, wherein the electric power is supplied to the scanning signal driving circuit and the video signal driving circuit of the front-stage display portion ARf side through a power supply switch 10f, while the electric power is supplied

to the scanning signal driving circuit and the video signal driving circuit of the back-stage display portion ARb side through a power supply switch 10b.

According to the liquid crystal display device having such a constitution, in the liquid crystal display portion AR, while of course the display can be performed over the whole area, the display may be performed only at the front-stage display portion ARf or the display may be performed only at the back-stage display portion ARb.

From the above description, when the liquid crystal display device of this embodiment is used as a liquid crystal display device in a portable telephone, for example, a mode in which information such as date, time, sensitivity of antenna and the like (information that can be displayed on a portion of the panel) is displayed as images at the front-stage display portion ARf and the back-stage display portion ARb is not driven can be realized.

Accordingly, the liquid crystal display device can be configured not to supply the electric power to respective gate signal lines GL of the back-stage display portion ARb so that the lowering of the power consumption can be effectively enhanced.

<<Constitution of pixel>>

Fig. 3 is a plan view which shows one embodiment of the pixel. This drawing particularly shows the pixel at a portion

where the drain signal lines DL are separated. That is, the drawing shows a portion of the upper-side pixel and a portion of the lower-side pixel with respect to the gate signal line GL which intersects the drain signal line DL. Fig. 4 is a cross-sectional view taken along a line IV-IV in Fig. 3.

In Fig. 3, first of all, a semiconductor layer AS which is made of poly-Si is formed on an upper surface of the transparent substrate SUB1 at a region where a thin film transistor TFT is formed.

A first insulation film GI which is made of SiO_2, for example, is formed over the transparent substrate SUB1 such that the first insulation film GI also covers the semiconductor layer AS.

This first insulation film GI functions as a gate insulation film in the region where the thin film transistor TFT is formed and functions as a dielectric film in a region where a capacitive element Cstg which will be explained later is formed.

The gate signal line GL is formed on the surface of the insulation film GI such that the gate signal line GL is extended in the x direction in the drawing. This gate signal line GL is formed such that a portion thereof is extended into the pixel region and is astride the semiconductor layer AS thus forming a gate electrode GT of the thin film transistor TFT.

Further, a storage line SL is formed simultaneously with

the formation of the gate signal line GL. The storage line SL is arranged substantially parallel to the gate signal line GL and an extension portion having a relatively large area is defined between the storage line SL and the gate signal line GL.

This extension portion of the storage line SL is configured to form one of electrodes of the capacitive element Cstg.

Then, a second insulation film IN which is for example made of SiO_2 is formed over the surface of the transparent substrate SUB1 such that the second insulation film IN also covers the gate signal line GL and the storage line SL.

This second insulation film IN functions as an interlayer insulation film of the drain signal line DL which will be explained later with respect to the gate signal line GL and also functions as a dielectric film in the region where the capacitive element Cstg is formed.

Further, contact holes CH1, CH2 are formed in the second insulation film IN such that these contact holes CH1, CH2 penetrate and reach the first insulation film GI which constitutes the lower layer so that portions of the drain region and the source region of the thin film transistor TFT are respectively exposed.

Then, the drain signal line DL which is extended in the y direction in the drawing is formed on the upper surface of

the second insulation film IN and the source electrode SD2 is formed on the upper surface of the second insulation film IN simultaneously with the drain signal line DL.

The drain signal line DL is formed such that the drain signal line DL runs over the contact hole CH1. Due to such a constitution, the drain signal line DL of the contact hole CH1 portion also acts as the drain electrode SD1 of the thin film transistor TFT.

Further, the drain signal line DL is separated on the gate signal line GL, wherein a separated end portion of one side of the drain signal line DL and a separated end portion of the other side of the drain signal line DL are both superposed on the gate signal line GL.

Such a provision is adopted to prevent the leaking of external light (such as light from the backlight) by shielding with the gate signal line GL. In other words, the light shielding of the cut portion of the drain signal line DL is performed by the gate signal line GL.

Further, the source electrode SD2 is formed such that the source electrode SD2 covers the contact hole CH2. The source electrode SD2 is also provided with an extension which is superposed on a portion of the storage line SL and an extension thereof.

The extension of the source electrode SD2 constitutes one electrode of the capacitive element Cstg.

Then, a third insulation film PSV which is made of SiO_2, for example, is formed over the transparent substrate SUB such that the third insulation film PSV also covers the drain signal line DL and the source electrode SD2. This third insulation film PSV functions as a protective film which prevents liquid crystal from being brought into direct contact with the thin film transistor TFT.

Further, a contact hole CH3 which exposes a portion of the extension of the source electrode SD2 is formed in the third insulation film PSV.

Still further, a pixel electrode PX which is made of ITO (indium-tin-oxide), for example, is formed on an upper surface of the third insulation film PSV such that the pixel electrode PX also covers the contact hole CH3.

<<Constitution of the memory>>

Fig. 5 is a plan view showing a portion of the above-mentioned memory shown in Fig. 1 corresponding to 1 bit. Further, Fig. 6 is a cross-sectional view taken along a line VI-VI of Fig. 5.

Further, the memory at this portion is a so-called dynamic memory and scale size circuit diagram thereof is shown in Fig. 7. The constitution shown in Fig. 5 substantially matches the scale circuit shown in Fig. 7 with respect to the geometric arrangement.

The memory shown in Fig. 5 is formed along with the

formation of the above-mentioned pixels.

As shown in Fig. 5, first of all, a semiconductor layer AS_1 and a semiconductor layer AS_2 which are made of poly-Si are formed on a surface of a transparent substrate SUB1. Among these semiconductor layers, the semiconductor layer AS_1 is used as a semiconductor layer which is part of a thin film transistor TFT_1 and the semiconductor layer AS_2 is used as a semiconductor layer which constitutes a thin film transistor TFT_2 and a thin film transistor TFT_3. These semiconductor layers AS_1, AS_2 are simultaneously formed with the formation of the semiconductor layer AS of the thin film transistor TFT in the liquid crystal display portion AR.

Then, a first insulation film GI which is made of SiO_2 is formed on an upper surface of the transparent substrate SUB such that the first insulation film GI also covers these semiconductor layers AS_1, AS_2. This first insulation film GI functions as gate insulation films of the thin film transistors TFT_1 to TFT_3.

A gate wiring layer Gl and a refresh wiring layer Rl which are extended in the x direction in the drawing are formed on an upper surface of the first insulation film GI. The gate wiring layer Gl and the refresh wiring layer Rl are simultaneously formed with the formation of the gate signal line GL in the liquid crystal display portion AR.

In this case, the gate wiring layer Gl is formed such

that the gate wiring layer G1 transverses a portion of the semiconductor layer AS_1 thus forming a gate electrode of the thin film transistor TFT_1, while the refresh wiring layer R1 is formed such that the refresh wiring layer R1 transverses a portion of the semiconductor layer AS_2 thus forming a gate electrode of the thin film transistor TFT_3.

A second insulation layer IN which is made of SiO_2 is formed on the upper surface of the transparent substrate SUB such that the second insulation layer IN also covers the gate wiring layer G1 and the refresh wiring layer R1.

The second insulation film IN functions as an interlayer insulation film for the gate wiring layer G1 and the refresh wiring layer R1 with respect to a drain wiring layer D1 which will be explained later.

Further, a drain region and a source region of the thin film transistor TFT_1, a source region of the thin film transistor TFT_2, and a drain region and a source region of the thin film transistor TFT_3, a portion of the refresh wiring layer R1, and a portion of a gate electrode GT3 are exposed by contact holes CH4, CH5, CH6, CH7, CH8 and CH9 through the second insulation film IN.

The drain wiring layer D1 which is extended in the y direction is formed on an upper surface of the second insulation film IN and this drain wiring layer D1 is connected to the drain region of the thin film transistor TFT_1 and the drain region

of the thin film transistor TFT_3. This drain wiring layer Dl is simultaneously formed with the drain signal line DL in the liquid crystal display portion AR.

Further, at this point of time, the gate electrode GT3 which is simultaneously formed with the gate wiring layer Gl is formed such that the gate electrode GT3 transverses the semiconductor layer AS_2 of the thin film transistor TFT_2. The gate electrode GT3 is connected to the source region of the thin film transistor TFT_1. Further, a conductive layer Cl which is simultaneously formed with the drain wiring layer Dl is also formed such that the conductive layer Cl establishes the connection between the source region of the thin film transistor TFT_2 and the refresh wiring layer Rl.

A third insulation film PSV which is made of SiO_2 is formed on the upper surface of the transparent substrate SUB such that the third insulation film PSV also covers the drain wiring layer Dl, the gate electrode GT3 and the conductive layer Cl. The third insulation film functions as an insulation film for protecting the thin film transistors TFT_1 to TFT_3.

Then, the conductive layer CL which is made of an ITO (Indium-Tin-Oxide) film is formed on an upper surface of the third insulation film PSV. The conductive layer CL is formed simultaneously at the time of forming the pixel electrodes PX in the liquid crystal display portion AR.

In this embodiment, the conductive layer CL is formed

such that the conductive layer CL covers the gate region of the thin film transistor TFT_2. However, the conductive layer CL is not limited to such a constitution and the conductive layer CL may be formed such that the conductive layer CL covers the respective gate regions of other thin film transistor TFT_1, TFT_3.

Here, the conductive layer CL is held at a fixed potential such as a ground potential, a power supply potential or the like.

The memory having such a constitution can be increased in storage capacity so that it becomes possible to obtain an advantageous effect that a margin of time beyond that necessary for holding the memory before which there is no leakage of current is generated in the respective thin film transistors TFT_1 to TFT_3.

«Explanation of manner of operation of the memory»

Fig. 8(a) is a view which shows the manner of operation of the dynamic memory, wherein (1) resetting of data lines (drain wiring layers) to a ground (GND), (2) data reading operation, (3) rewriting of data and (4) writing of new data are respectively indicated by the flow of electric current.

Further, Fig. 8(b) indicates timing charts of respective signals.

«Liquid crystal display panel»

Fig. 9 is a view which shows the relationship between a liquid crystal display panel PNL which uses a transparent

substrate SUB1 and a substrate SUB2 which are arranged to face each other with liquid crystal LC inserted between them, the substrates acting as an envelope and a backlight BL which is arranged at the back surface of the liquid crystal display panel (with respect to an observer).

A polarization film POL2 is formed on the surface of the transparent substrate SUB1 opposite to the liquid crystal, while a polarization film POL1 is formed on a surface of the transparent substrate SUB2 opposite to the liquid crystal. The transparent substrate SUB2 is fixedly secured to the transparent substrate SUB1 by a sealing agent SL which also has a function of sealing liquid crystal between the transparent substrates SUB1 and SUB2.

Light from the backlight BL is irradiated to an observer through the liquid crystal LC in which the light transmittivity of respective pixels in the liquid crystal display portion AR of the liquid crystal display panel PNL is controlled.

In this case, a light shielding film BT is formed on a backlight (BL) side of the transparent substrate SUB1 and this light shielding film BT prevents the light irradiated from the backlight BL from being irradiated to at least the H-side address decoder, the input data take-in (output) circuit and the memory shown in Fig. 1 respectively.

However, it is needless to say that the light shielding film BT may be formed on the whole peripheral region of the liquid

crystal display portion AR (region formed of the mass of the pixels), only opening the liquid crystal display portion AR.

The liquid crystal display panel PNL which has such a constitution can prevent the light from the backlight BL from being irradiated to respective thin film transistors TFT_1 to TFT_3 which constitute the dynamic memory so that it becomes possible to obtain an advantageous effect that the occurrence of erroneous operations can be avoided. That is, when the dynamic memory is used, the adverse influence derived from photons generated in the semiconductors due to the irradiation of light is extremely large. The liquid crystal display panel PNL can overcome such a problem.

In this embodiment, the circuits such as the dynamic memory and the like are formed on the liquid-crystal side of the transparent substrate SUB1 which is opposite the backlight BL. However, it is needless to say that these circuits may be formed on the other transparent substrate SUB2.

This is because that such a constitution in this case also can prevent the irradiation of the external light to the dynamic memory. A black vinyl film or the like, for example, may be used as the light shielding film BT.

<<Driving method of liquid crystal display panel>>

Fig. 10 shows a driving method of the liquid crystal display panel PNL, and more particularly, a driving method of pixel driving shift registers 1f, 1b and a method for

transmitting video signals from the video signal driving circuit which becomes necessary along with the driving method of the liquid crystal display panel PNL.

As mentioned previously, according to the liquid crystal display device of this embodiment, the liquid crystal display portion AR is divided into the front-stage display portion ARf and the back-stage display portion ARb and the scanning signals are supplied to the gate signal lines GL through the separate pixel driving shift registers 1f, 1b respectively.

Then, as an example of such a driving, the scanning signals are supplied to respective gate signal lines GL in the directions (directions A) moving away from the gate signal line GL of the front-stage display portion ARf side and the gate signal line GL of the back-stage display portion ARb side which are present at the boundary of the front-stage display portion ARf and the back-stage display portion ARb.

Further, as another example, as an opposite case, it may be possible that the scanning signals are sequentially supplied to respective gate signal lines GL along directions (directions B) which approach the boundary between the front-stage display part ARf and the back-stage display part ARb. That is, the scanning signal lines are firstly supplied to the gate signal line GL of the front-stage part ARf side and the gate signal line GL of the back-stage part ARb side which are disposed remotest from the boundary and then are sequentially supplied

to other gate signal lines GL of the front-stage part ARf side and other gate signal lines GL of the back-stage part ARb side along the directions B.

With such a constitution, it becomes possible to obtain an advantageous effect that the display at the boundary between the front-stage display portion ARf and the back-stage display portion ARb becomes extremely natural. That is, with respect to pixels of the front-stage display portion ARf at the boundary and pixels of the back-stage display portion ARb at the boundary, the time difference between their driving can be minimized so that the leaking of current becoming large at pixels on one side, for example, can be eliminated.

Although the embodiments which adopt the liquid crystal display device as the display device have been described heretofore, the constitution of the present invention is applicable to other display device such as an organic EL, an OLED or the like without departing from the spirit of the present invention.

As can be clearly understood from the above-mentioned description, according to the display device of the present invention, it becomes possible to obtain the display device with little power consumption.

Further, the leak current which is generated in the thin film transistors which constitute the dynamic memory in the inside of the video signal driving circuit can be suppressed.

Further, it becomes possible to normally operate the dynamic memory in the inside of the video signal driving circuit.